Electronic Version
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Claims

[c1] A method of fabricating a semiconductor structure, comprising the steps of:
forming a raised source region on a substrate;
forming a raised drain region on the substrate; and
forming a first silicon layer over the raised source region and a second silicon layer over the raised drain region.

[c2] A method according to claim 1, wherein the substrate includes a SiGe layer atop a buried oxide layer.

[c3] A method according to claim 1, further comprising a step of forming a gate stack on the substrate.

[c4] A method according to claim 3, further comprising a step of forming a trench isolation surrounding the gate stack, source region and drain region.

[c5] A method according to claim 1, further comprising a step of forming a first silicide contact on the first silicon layer.

[c6] A method according to claim 1, further comprising a step of forming a second silicide contact on the second silicon layer.

[c7] A method according to claim 1, wherein the first silicon layer is epitaxially formed silicon and the second silicon layer is epitaxially grown silicon.

[c8] A method according to claim 1, wherein the raised drain region is comprised of a strained silicon layer atop a SiGe layer.

[c9] A method according to claim 8, wherein the strained silicon layer is comprised of epitaxially grown silicon.

[c10] A method according to claim 1, wherein the raised source region is comprised of a strained silicon layer atop a SiGe layer.

[c11] A method according to claim 10, wherein the strained silicon layer is comprised of epitaxially grown silicon.

[c12] A method according to claim 1, wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions and sidewall portions, the method further comprising a step of forming sacrificial spacers along the silicon sidewall portions.

[c13] A method according to claim 12, further comprising steps of:
forming a third silicon layer over the cap of the first sili-

con layer over the raised source region; and
forming a fourth silicon layer over the cap of the second silicon layer over the raised drain region.

[c14] A method according to claim 13, further comprising a step of removing the sacrificial spacers.

[c15] A method according to claim 14, wherein the step of removing the sacrificial spacers includes etching away the sacrificial spacers.

[c16] A semiconductor structure, comprising:
a substrate;
a raised source region on the substrate;
a raised drain region on the substrate; and
a first silicon layer over the raised source region and a second silicon layer over the raised drain region.

[c17] A semiconductor structure according to claim 16, wherein the substrate includes a SiGe layer atop a buried oxide layer.

[c18] A semiconductor structure according to claim 16, further comprising a gate stack on the substrate.

[c19] A semiconductor structure according to claim 18, further comprising a trench isolation surrounding the gate stack, source region and drain region.

[c20] A semiconductor structure according to claim 16, further comprising a a first silicide contact on the first silicon layer.

[c21] A semiconductor structure according to claim 16, further comprising a second silicide contact on the second silicon layer.

[c22] A semiconductor structure according to claim 16, wherein the first silicon layer is epitaxially formed silicon and the second silicon layer is epitaxially grown silicon.

[c23] A semiconductor structure according to claim 1, wherein the raised drain region is comprised of a strained silicon layer atop a SiGe layer.

[c24] A semiconductor structure according to claim 23, wherein the strained silicon layer is comprised of epitaxially grown silicon.

[c25] A semiconductor structure according to claim 1, wherein the raised source region and the raised drain region are comprised of a strained silicon layer atop a SiGe layer.

[c26] A semiconductor structure according to claim 1, wherein the first silicon layer formed over the raised source region and the second silicon layer over the raised drain region include cap portions and sidewall portions, the

semiconductor structure further comprising sacrificial spacers along the silicon sidewall portions.

[c27] A semiconductor structure according to claim 26, further comprising:
a third silicon layer over the cap of the first silicon layer over the raised source region; and
a fourth silicon layer over the cap of the second silicon layer over the raised drain region.

[c28] A semiconductor structure according to claim 27, wherein the sacrificial spacers have been removed.